SPECIFICATION

[◉] Preliminary Specification
[ ] Final Specification

Description **7” TFT-LCD Module**

Part Number SW070FHD-2000

Customer				
Signatures	Date		Approved By	Date
				2022/09/20
			Reviewed By	
				2022/09/20
			Prepared By	
				2022/09/20
Comments:				

REVISION HISTORY

Rev	Date	Page	Revision Items	Editor
1.0	2022/09/20	-	First release	Yang Yang

CONTENTS

1. Summary

1.1 General Description

This is a 7 inch LTPS-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module with normal-black technology.It is composed of a TFT-LCD panel, LCD Driver IC with T-con integrated, POL,FPC, cover glass and a LED backlight unit.

1.2 Features

- Ultra-wide viewing angle
- High resolution 1920(H) ×RGB×1080(V)
- Interface: MIPI
- Compliant with the European RoHS Directive (2011/65/EU) and Delegated Directive (2015/863/EU, Amending Annex II of 2011/65/EU)

2. General Specifications

Feature		Spec	Unit
Display Spec	Size	7 inches	
	Resolution	1920(H) ×RGB×1080(V)	
	Pixel Pitch	0.0804x0.0804	mm
	TFT Active Area	154.368X86.832	mm
	Technology Type	LTPS	
	Pixel Configuration	R.G.B Vertical Stripe	
	Display Mode	SFT	
	Surface Treatment	HC	
	Viewing Direction	All direction	
	Gray Scale Inversion Direction	NA	
Mechanical Characteristics	LCM (W x H x D)	163.73x91.33x2.36	mm
	Weight	72.5	g
Optical Characteristics	Luminance	2000	cd/m^2
	Contrast Ratio	1000:1	
	NTSC	80	%
	Viewing Angle	88/88/88/88	degree
Electrical Characteristics	Interface	MIPI	
	Color Depth	16.7 Million	color
	Power Consumption	LCD:TBD	mW

Table 2.1 General TFT Specifications

3. Input / Output Terminals

3.1 CN1 Pin assignment (LCD Interface)

Connector Information	
LCD Module connector	FH35C-39S-0.3SHW

Table 3.1.1 Connector information

No	Symbol	I/O	Description	Comment
1	GND	P	GND	
2	LED_K3	P	LED Cathode	NC
3	LED_K2	P	LED Cathode	NC
4	LED_K1	P	LED Cathode	NC
5	NC	N	No connection	
6	LED_A	P	LED Anode	NC
7	NC	N	No connection	
8	AVEE	P	Power Supply, -5.5V	
9	AVEE	P	Power Supply, -5.5V	
10	NC	N	No connection	
11	AVDD	P	Power Supply, 5.5V	
12	AVDD	P	Power Supply, 5.5V	
13	NC	N	No connection	
14	VDDI	P	Power Supply, 1.8V	
15	NC	N	No connection	
16	LCD_RST	I	Reset pin for display	
17	TP_RST	I	reset pin for touch	
18	TP_INT	O	Touch screen interrupt line	
19	TP_SDA	I/O	I2C interface data pin for touch	
20	TP_SCL	I	I2C interface clock pin for touch	
21	GND	P	GND	
22	CABC_PWM	O	LCD backlight control.	
23	TE	O	Tearing Effect output signal	
24	GND	P	GND	
25	D3N	I	Negative MIPI_DSI Data differential signal input pin	
26	D3P	I	Positive MIPI_DSI Data differential signal input pin	
27	GND	P	GND	
28	D0N	I/O	Negative MIPI_DSI Data differential signal input and output pin	
29	D0P	I/O	Positive MIPI_DSI Data differential signal input and output pin	
30	GND	P	GND	
31	CLKN	I	Positive MIPI_DSI clock differential signal input pin	
32	CLKP	I	Negative MIPI_DSI clock differential signal input pin	
33	GND	P	GND	

34	D1N	I	Negative MIPI_DSI Data differential signal input pin	
35	D1P	I	Positive MIPI_DSI Data differential signal input pin	
36	GND	P	GND	
37	D2N	I	Negative MIPI_DSI Data differential signal input pin	
38	D2P	I	Positive MIPI_DSI Data differential signal input pin	
39	GND	P	GND	

Table 3.1.2 Pin Assignment for LCD Interface

Note1: I/O definition: I---Input, O---Output, P---Power/Ground, N---No connection
Note2: All of the GND pins should be connected to the system ground.

4. Absolute Maximum Ratings

Item	Symbol	MIN	MAX	Unit	Remark
LCD logic Voltage	IOVCC	-0.3	1.95	V	
LCD Analog Voltage	VSP	-0.3	6.3	V	
LCD Analog Voltage	VSN	-6.3	0.3	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	
Relative Humidity Note2	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃＜Ta≤50℃
		--	≤55	%	50℃＜Ta≤60℃
		--	≤36	%	60℃＜Ta≤70℃
		--	≤24	%	70℃＜Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m³	Ta＞70℃

Table 4.1 Absolute Maximum Ratings

Note1: Input voltage include all in put data.
Note2: Ta means the ambient temperature. It is necessary to limit the relative humidity to the specified temperature range. Condensation on the module is not allowed.
Note3: The absolute maximum rating values of this product are not allowed to be exceeded at any times. A module should be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme condition, the module may be permanently destroyed

5. Electrical Characteristics

5.1 DC Characteristics for Panel Driving

Item		Symbol	MIN	TYP	MAX	Unit	Remark
LCD Input Analog Voltage		VSP-Vss	5.4	5.5	5.6	V	
		VSN-Vss	-5.6	-5.5	-5.4	V	
LCD Logic I/O Voltage		IOVCC-Vss	1.7	1.8	1.9	IOVCC-Vss	
"H" Level Input Voltage		VIH	0.7xIOVCC	-	IOVCC	VIH	
"L" Level Input Voltage		VIL	VSS	-	0.3xIOVCC	VIL	
"H" Level Output Voltage		VOH	0.8xIOVCC	-	IOVCC	VOH	
"L" Level Output Voltage		VOL	0.0	-	0.2xIOVCC	VOL	
Power Consumption	60Hz	P	--	TBD	--	mW	Black pattern

Table 5.1.1 Operating Voltages

Note1: Indicated the subsequent version may be updated.

5.2 Logic Power Consumption

Parameter	Symbol	Values		Units	Notes
		Typ	Max		
Normal Mode	I_{IOVCC}	TBD		**mA**	**White Pattern (no touch)**
	I_{Vsp}	TBD		**mA**	
	I_{Vsn}	TBD		**mA**	
Sleep Mode	I_{IOVCC}	TBD		**uA**	
	I_{Vsp}	TBD		**uA**	
	I_{Vsn}	TBD		**uA**	

5.3 Recommended Power ON/OFF Sequence

1.1 Normal mode

The power sequence of normal mode

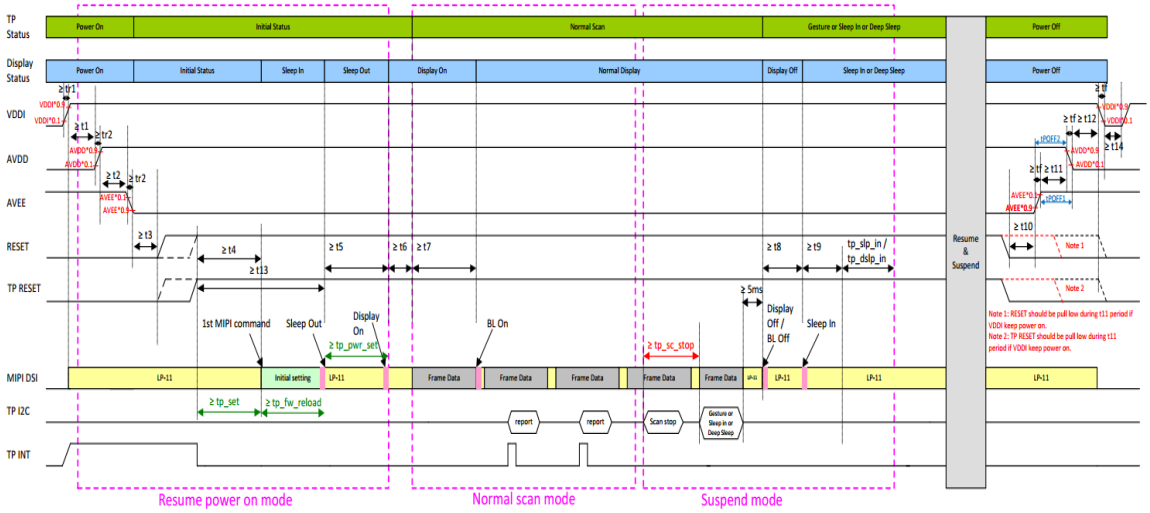
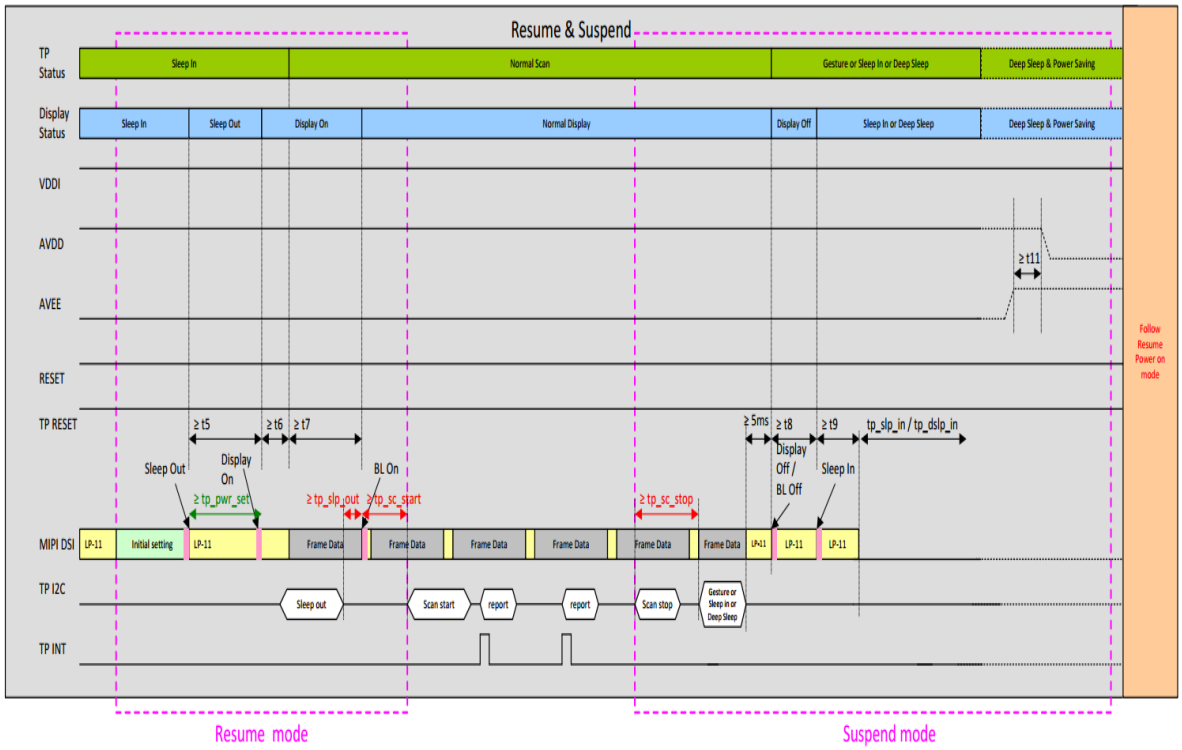
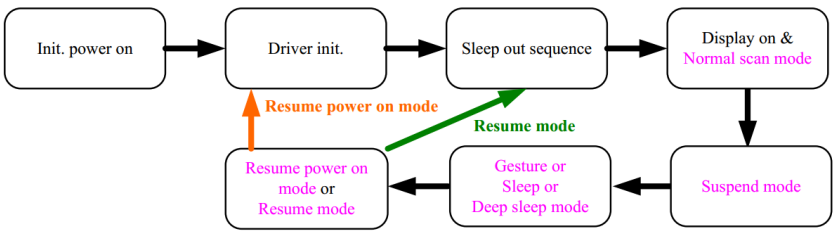


Figure 5.2.1 Power on sequence



The flow chart of normal mode



Normal Mode	Min.	Typ.	Max.	Note
tr1 (ms)	0.05	-	20	VDDI rising time
tr2 (ms)	0.05	-	20	AVDD, AVEE rising time
tf (ms)	0.05	-	20	External power falling time
t1 (ms)	1	-	-	
t2 (ms)	1	-	-	
t3 (ms)	1	-	-	
t4 (ms)	10	-	-	DDI OTP reload. RESET to first command in display sleep in mode time.
t5 (ms)	60	-	-	Sleep Out Sequence
t6 (ms)	0	-	-	
t7 (ms)	50	-	-	
t8 (ms)	16.67	-	-	Depend on frame rate.
T9 (ms)	80	-	-	Sleep In Sequence *The min. time of sleep in should be longer than panel power off request
t10 (ms)	1	-	-	
t11 (ms)	0	-	-	AVDD≧|AVEE| *No limitation for t11
tPOFF2 (ms)	0.05	-	-	AVEE 90% to AVDD 90%
tPOFF1 (ms)	0.05	-	-	AVEE 10% to AVDD 10%
t12 (ms)	0	-	-	
t13 (ms)	47	-	-	TP RESET to 1st TP CMD delay time
t14(ms)	10	-	-	Delay time between VDDI power off to power on
tp_set (ms)	10	-	-	TP OTP reload
tp_fw_reload (ms)	37	-	-	Flash reload
tp_pwr_set (ms)	60	-	-	Initial setting
tp_slp_out (ms)	0	-	-	Resume timing
tp_sc_start (ms)	35	-	-	
tp_sc_stop (ms)	35	-	-	
tp_slp_in (ms)	35	-	-	Entry Sleep mode wait time
tp_dslp_in (ms)	35	-	-	Entry Deep Sleep mode wait time

*Resume Power On mode : If resume AVDD & AVEE power off, please follow Resume power on mode.

* When sleep in mode, RESET & TP RESET can keep low after AVDD & AVEE power off.

* Exit Deep Sleep mode : Entry deep sleep mode and AVDD & AVEE power off, please follow Resume power on mode.

Note1:The power on/off sequence is the first version. It will be updated when the design is fixed.

5.4 LCD Module Block Diagram

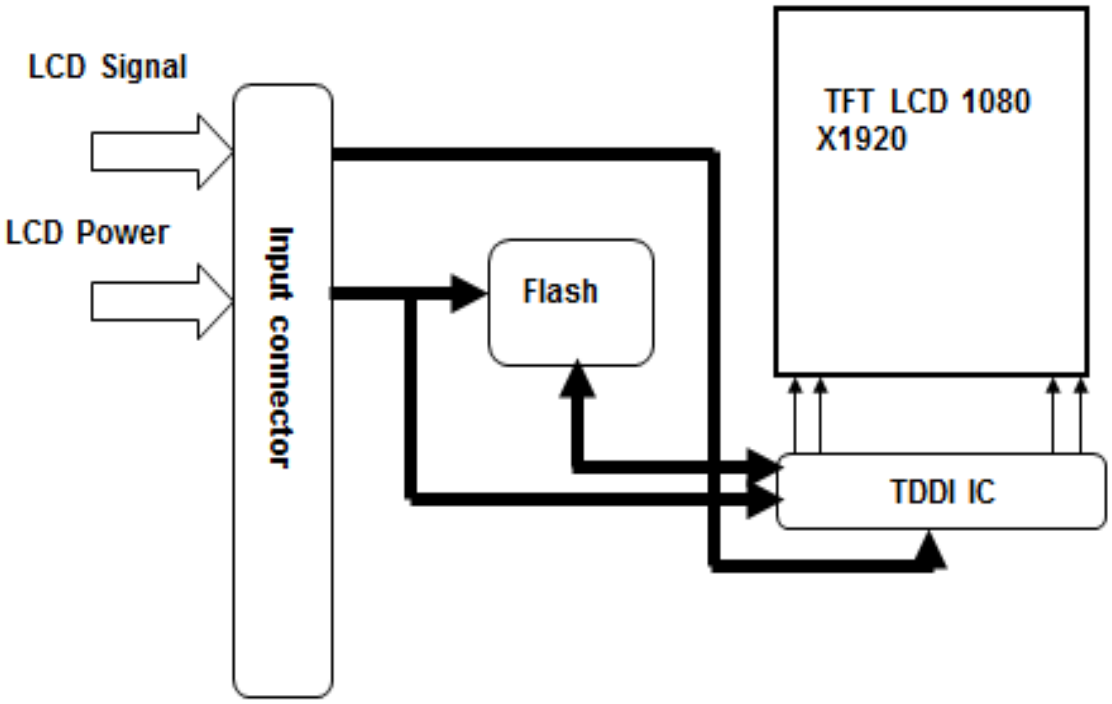


Figure 5.5.1 LCD Module Block Diagram

6. Timing Characteristics

6.1 AC characteristics

6.1.1 DC characteristic for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below. DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OHLP}	I_{OUT} = -1mA	0.8*VDDAM	-	VDDAM	V
Logic Low level output voltage	V_{OLLP}	I_{OUT} = 1mA	0.0	-	0.2*VDDAM	V
Logic High level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1, D2, D3)	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1, D2, D3)	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Note:

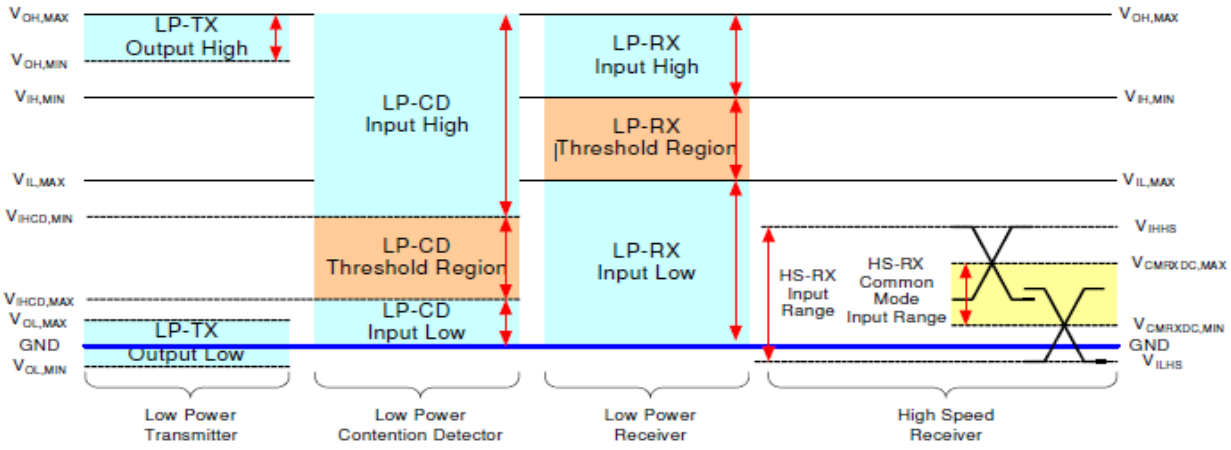
1. Ta=-30℃ to 70℃
2. This table only uses for DSI LP mode (DSI High Speed mode is off).

6.1.2 DC characteristics for DSI HS mode

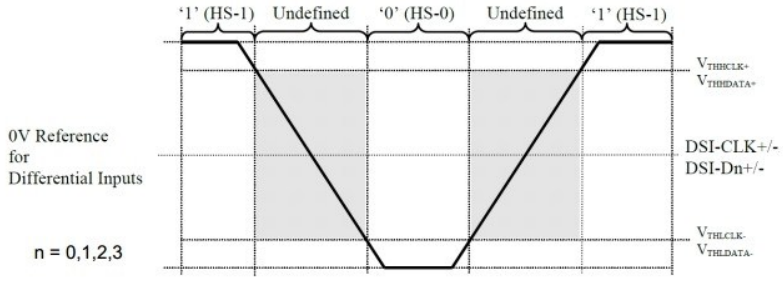
Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Note:

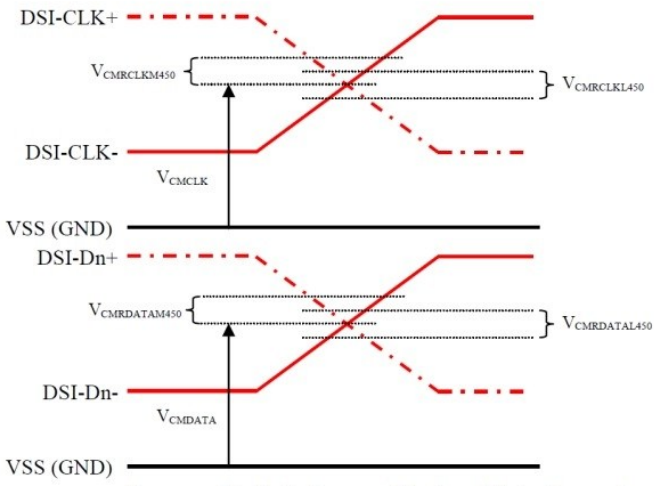
1. Ta = -30 to 70°C, VDDI=1.65V ~ 1.95V, AVDD=4.5V ~ 6.3V, AVEE=-4.5V ~ -6.3V, VSS=AVSS=0V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0,1,2,3
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.



The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.



Differential Inputs Logical '0's and '1's, Threshold High/Low, Differential Voltage Range

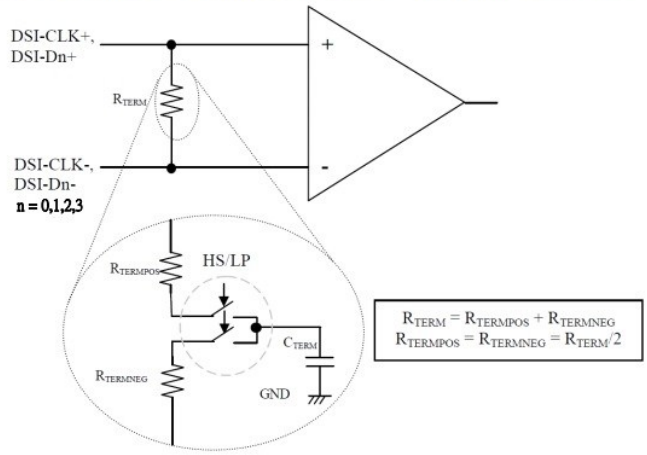


Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (DSI-CLK+ ⇔ DSI-CLK- or DSI-D0+ ⇔ DSI-D0- or DSI-D1+ ⇔ DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (DSI-CLK+ ⇔ DSI-CLK- or DSI-D0+ ⇔ DSI-D0- or DSI-D1+ ⇔ DSI-D1-)

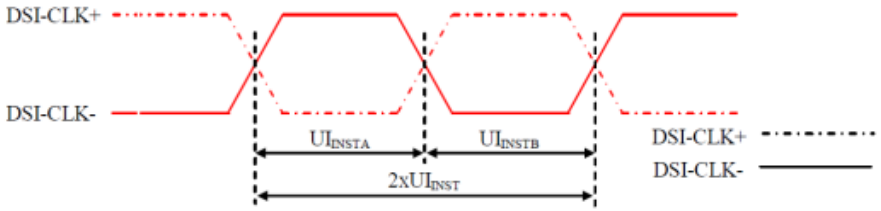
The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.



Differential Pair Termination Resistor on the Receiver Side

6.2 DSI AC characteristics

6.2.1 High Speed Mode-Clock Channel Timing



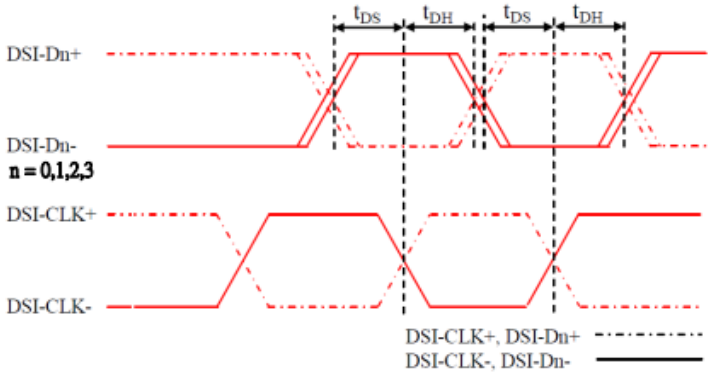
DSI Clock Channel Timing

DSI Clock Channel Timing

Signal	Symbol	Parameter	Min.	Max.	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	25	ns
DSI-CLK+/-	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	1	12.5	ns

Note: $UI_{INST} = UI_{INSTA} = UI_{INSTB}$

6.2.2 High Speed Mode-Data Clock Channel Timing

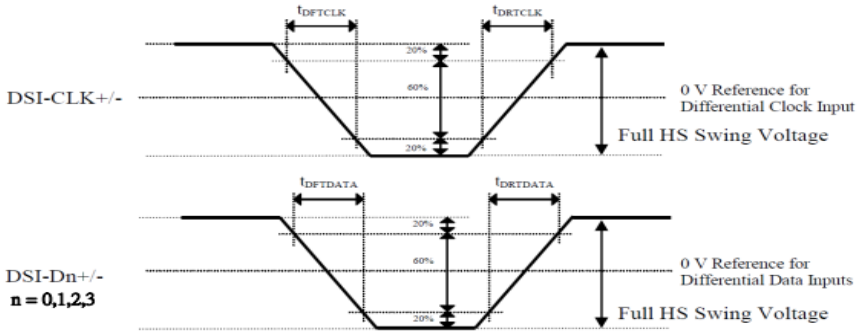


DSI Data to Clock Channel Timings

DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min.	Max.
DSI-Dn+/- (n=0,1,2,3)	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

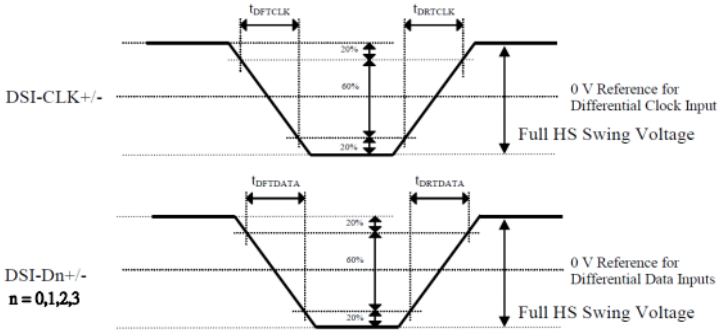
6.2.3 High Speed Mode-Rise and fall Timings



Rise and Fall Timings on Clock and Data Channels

Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min.	Typ.	Max.
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI



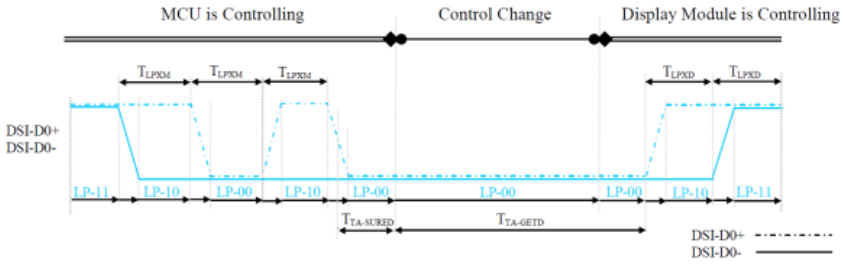
Rise and Fall Timings on Clock and Data Channels

Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min.	Typ.	Max.
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI

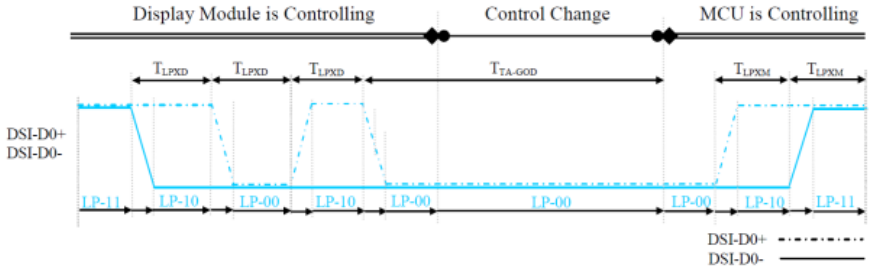
6.2.4 Low Speed Mode-Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MCU to the Display Module sequence below.



BTA from the MCU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module to the MCU sequence below.



BTA from the Display Module to the MCU

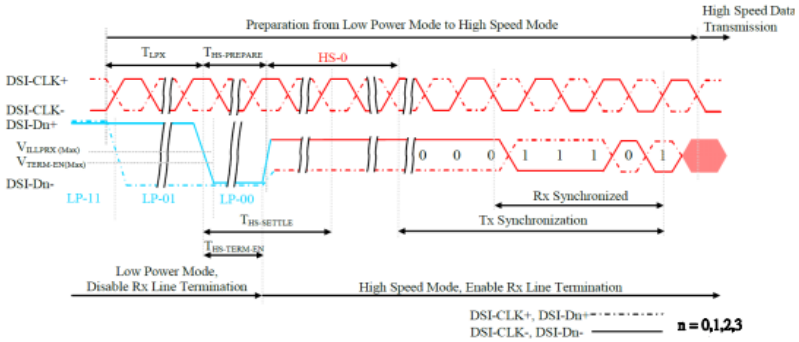
Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MCU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module starts driving	T_{LPXD}	$2*T_{LPXD}$	ns

Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module	$5*T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	$4*T_{LPXD}$	ns

6.2.5 Data Lanes from Low Power Mode to High Speed Mode

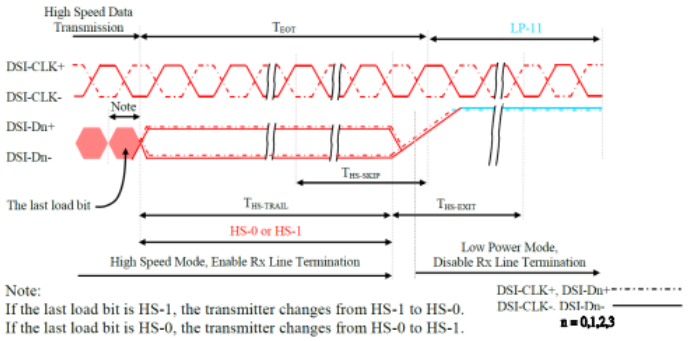


Data Lanes – Low Power Mode to High Speed Mode Timings

Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

6.2.6 Data Lanes from High Speed Mode to Low Power Mode

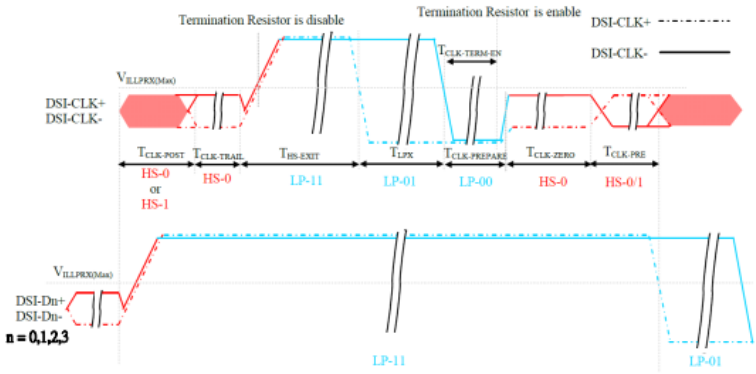


Data Lanes – High Speed Mode to Low Power Mode Timings

Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-SKIP}$	Time-Out at Display Module to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(8*UI, 60ns+4*UI)	-	ns

6.2.7 DSI Clock Burst-High Speed Mode to/from Low Power Mode

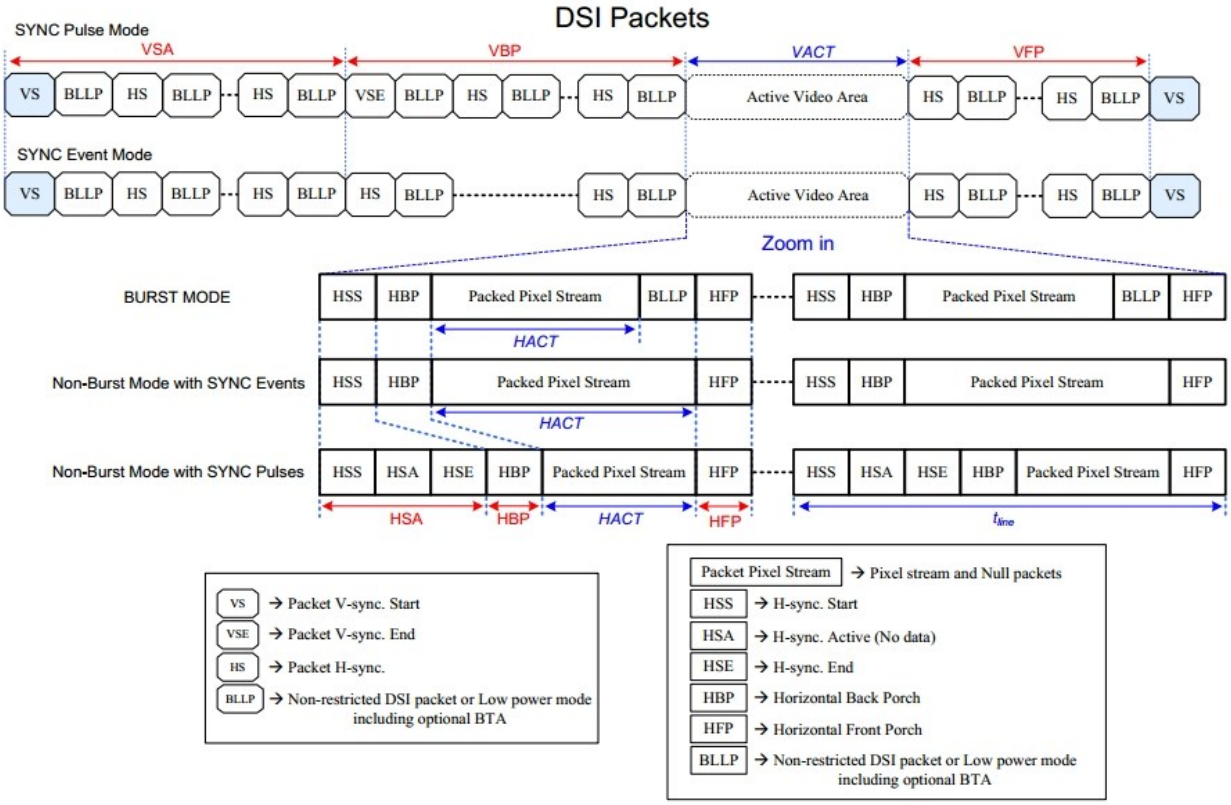


Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Clock Lanes – High Speed Mode to/from Low Power Mode Timings

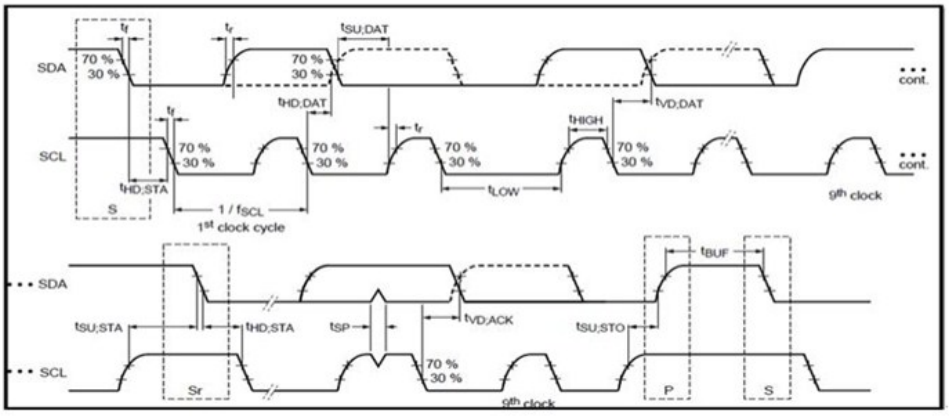
Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

6.3 Timing for DSI video mode

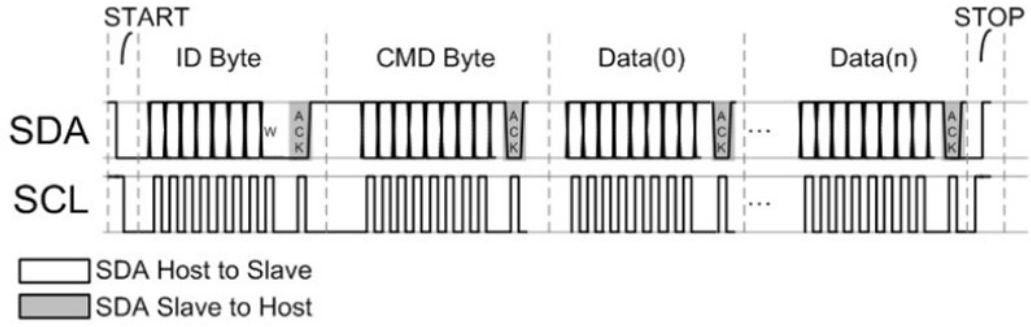


Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. Active	VSA Note 6, 7	2	-	-	Line
Vertical Back Porch	VBP Note 6, 7	6	-	-	Line
Vertical Front Porch	VFP Note 6, 7	30	-	-	Line
Active lines per frame	VACT	1280	1920	2520	Line
Horizontal sync. Active	HSA	2	-	-	Pixel
Horizontal Porch	HSA + HBP+ HFP	0.5	-		us
Active pixels per line	HACT	720	1080	1080	Pixel

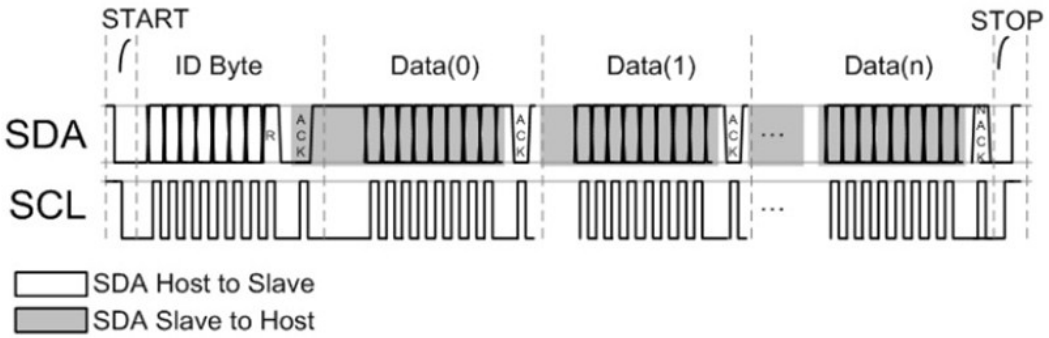
6.4 I2C Interface Timing



Parameter	Symbol	Fast-mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time START condition	$t_{HD:STA}$	0.6	-	us
LOW period of the SCL clock	t_{Low}	1.3	-	us
High period of the SCL clock	t_{High}	0.6	-	us
Set-up time for a repeated START condition	$t_{SU:STA}$	0.6	-	us
Data hold time	$t_{HD:DAT}$	100	-	ns
Data set-up time	$t_{SU:DAT}$	100	-	ns
Rise time of both SDA and SCL signals (30% to 70%)	t_r	-	300	ns
Fall time of both SDA and SCL signals (70% to 30%)	t_f	-	300	ns
Signal pulse glitch tolerance	t_{SP}	-	50	ns
Set-up time for STOP condition	$t_{SU:STO}$	0.6	-	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	us



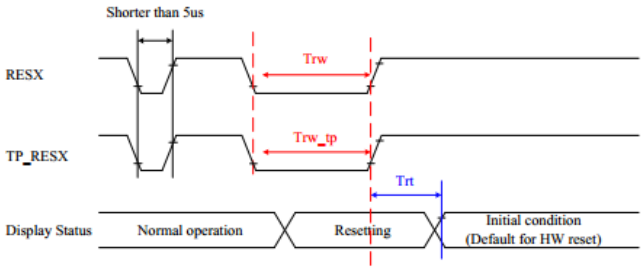
I2C protocol diagram (Write)



I2C protocol diagram (Read)

Note:SDA= TP_I2C_SDA,SCL= TP_I2C_SCL

6.5 Reset Input Timing



Reset Timing

Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	Trw	Reset pulse duration	10	-	us
	Trt	Reset cancel	35 (Note 1,5)	-	ms
			150 (Note 1,6,7)	-	ms
TP_RESX	Trw_tp	Reset pulse duration	10	-	us

Note:

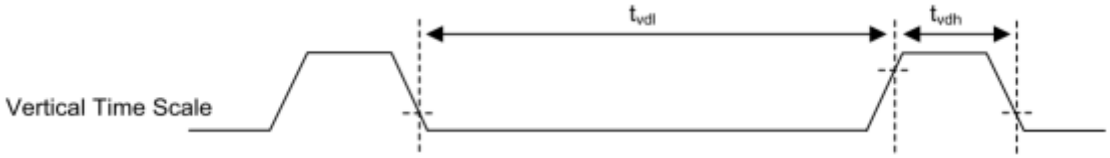
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM to registers. This loading is done every time when there is H/W reset cancel time (Trt) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table.

Reset Description

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Figure 6.5.1 Reset Input Timing

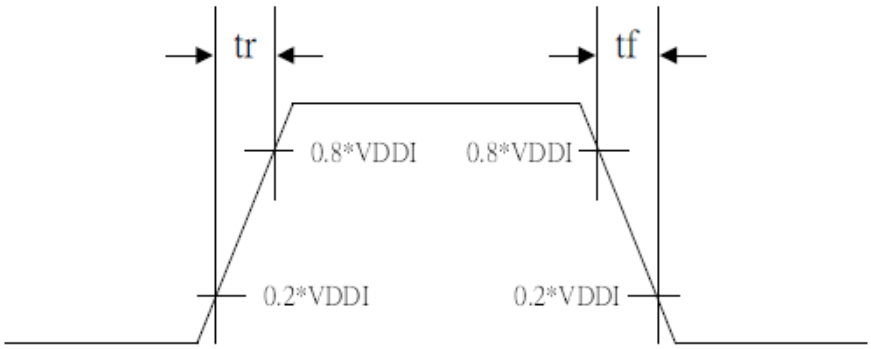
6.6 Tearing Effect Line Modes



The tearing effect output signal consists of V-sync information only.

- **t vdh = The LCD display is not updated.**
- **t vdl = The LCD display is updated (except Invisible line-see below).**

NOTE: During sleep in mode, the tearing effect output pin is low


tr
tf
0.8*VDDI
0.8*VDDI
0.2*VDDI
0.2*VDDI

7. Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	80	85		degree	Note2,3
		θB		80	85			
		θL		80	85			
		θR		80	85			
Contrast Ratio		CR	θ=0°	800	1000			Note 3
Response Time		T_{ON}	25℃	-	-	30	ms	Note 4
		T_{OFF}						
Chromaticity	**White**	x	Backlight is on	-	0.334	-		Note 1,5
		y		-	0.341	-		
	Red	x		-	0.641	-		Note 1,5
		y		-	0.335	-		
	Green	x		-	0.260	-		Note 1,5
		y		-	0.658	-		
	Blue	x		-	0.151	-		Note 1,5
		y		-	0.069	-		
Uniformity		U		75	80	-	%	Note 6
NTSC		-		75	80	-	%	Note 5
Luminance		L		800	1000	-	cd/m^2	Note 7

Table 7.1 Optical Parameters

Test Conditions:

1. I_F= **3*16.5**mA, and the ambient temperature is 25℃.
2. The test systems refer to Note1 and Note2.

Note1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical characteristics are measured at the center point of the LCD screen.

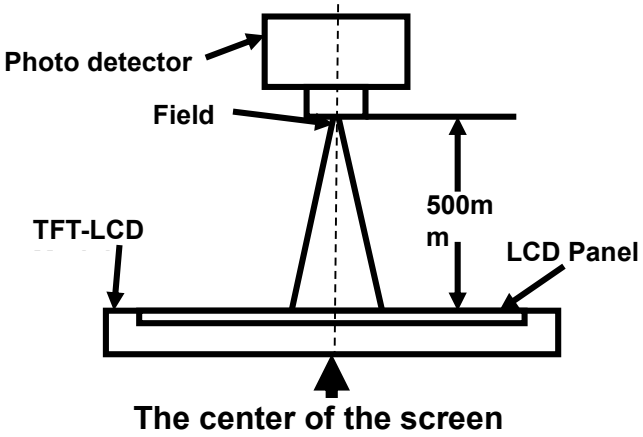


Fig1. Measurement Set Up

Note2: Definition of viewing angle range and measurement system. Viewing angle is measured at the center point of the LCD 。

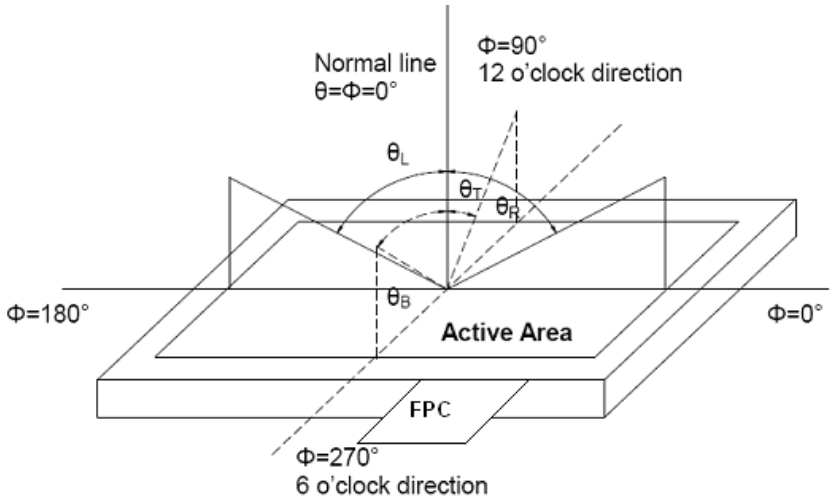


Fig2. Measurement viewing angle

Note3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note4: Definition of Response time

For TN LCM,the response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_r) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_f) is the time between photo detector output intensity changed from 10% to 90%.

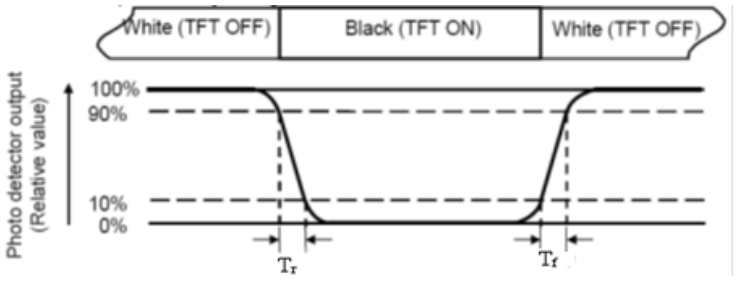


Fig3. Response Time Testing(TN)

For SFT LCM, the response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_r) is the time between photo detector output intensity changed from 10% to 90%. And fall time (T_f) is the time between photo detector output intensity changed from 90% to 10%.

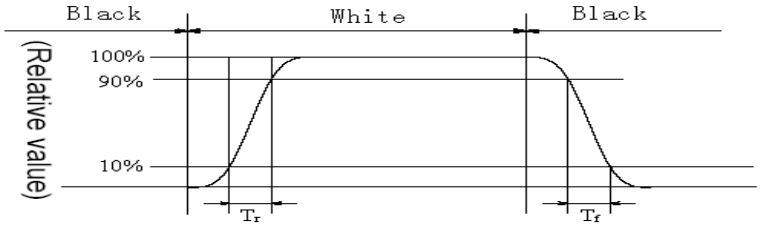


Fig4. Response Time Testing(SFT)

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig.5). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

L-------Active area length; W----- Active area width

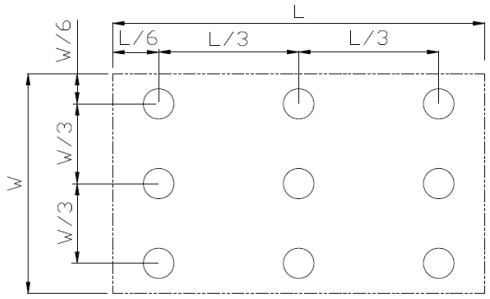


Fig5. Luminance Uniformity Measurement Locations(9 points)

Note7: Definition of Luminance:

Measure the luminance of white state at center point.

8. Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	+70℃，48H	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	-20℃，48H	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	+80℃，48H	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	-30℃，48H	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity(non-operation)	+60℃，90%RH，48H	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-30℃，30min~80℃，30min，change time：5min，20cycle	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	ESD	C=150pF，R=330Ω，5point/panel Air：±8kv，5times； Contact：±4kv，5times； （Environment：15℃~35℃，30%~60%，86Kpa~106Kpa）	IEC61000-4-2:2001 GB/T17626.2-2006
8	Package Vibration	5-20-200HZ，PSD：0.01-0.01-0.001 Total:0.781g2/HZ,x/y/z 30min）	
9	Package Drop Test	Height: X cm,1 corner, 3edges, 6 surfaces Note：X＞10Kg:60cm；≤10Kg:80cm	IEC60068-2-32:1990 GB/T2423.8—1995

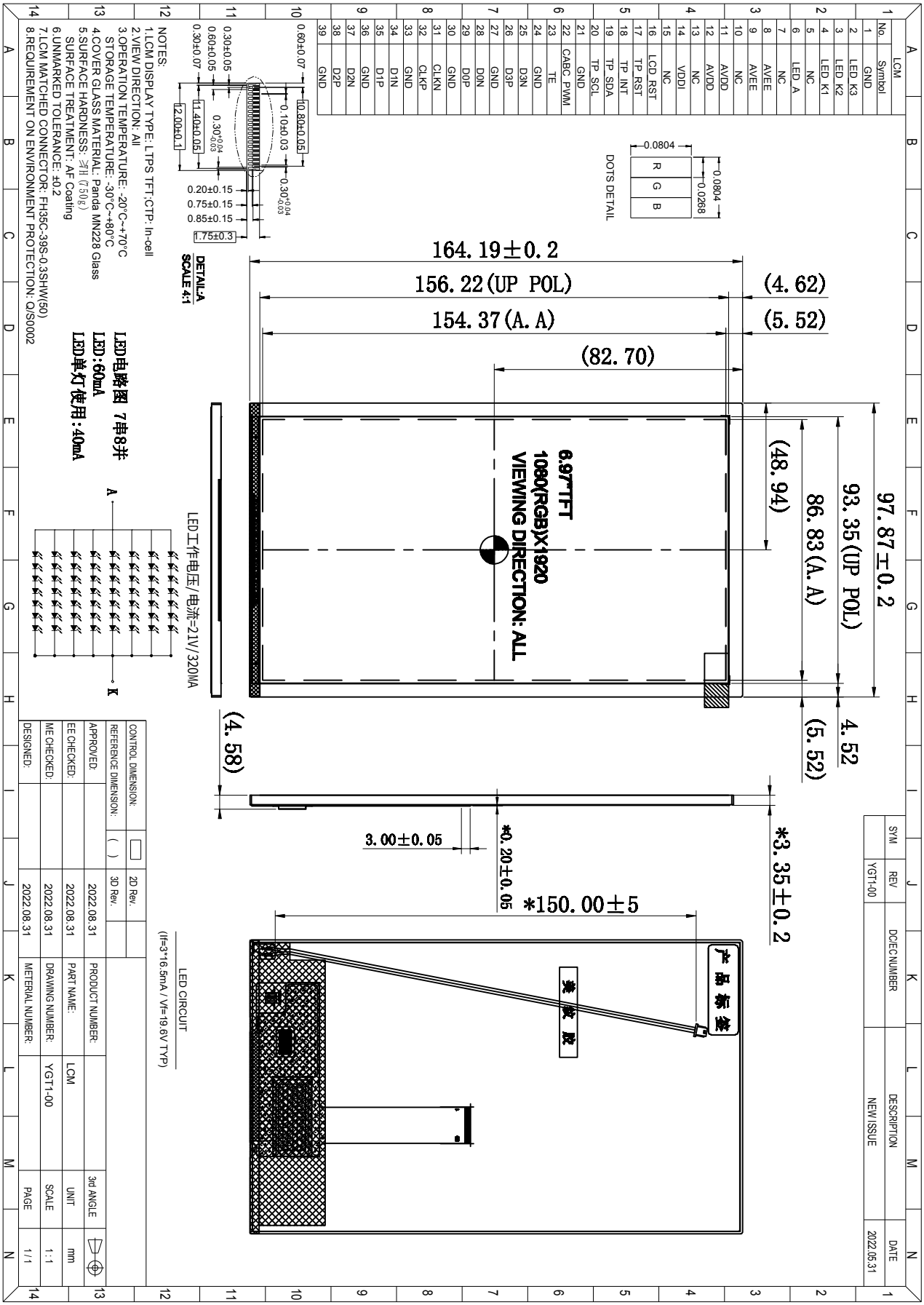
Table 8.1 RA test condition

Note1: Temperature is the ambient temperature of sample

Note2: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product's function only be guaranteed, but not for all of the cosmetic specification.

9. Mechanical Drawing



11. Precautions for Use of LCD Modules

11.1 Handling Precautions

(1) The display panel is made of glass. Do not subject it to mechanical shock by dropping it, etc.
(2) If the display panel is damaged and the liquid crystal fluid inside it leaks out be sure not to get any in your mouth. If the fluid comes into contact with your skin or clothes promptly wash it off using soap and water.
(3) Do not apply excessive force to the display surface or the bezel since this may cause the color tone to vary.
(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle the polarizer carefully.
(5) If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear use a moist cloth with one of the following solvents:
   — Isopropyl alcohol
   — Ethyl alcohol

   Solvents other than those mentioned above may damage the polarizer. Specifically, do not use the following:
   — Water
   — Ketone
   — Aromatic solvents
(6) Do not disassemble the LCD Module.
(7) If powered off, do not apply the input signals.
(8) To prevent destruction of the module by static electricity, be careful to maintain an optimum work environment.
(9) Be sure to ground your body when handling the LCD Modules.
(10) Tools used for assembly, must be properly grounded.
(11) To reduce the amount of static electricity generated, do not conduct assembly or other work under very low humidity conditions.
(12) The LCD Module is covered with a film to protect the display surface, remove film slowly under the ionizer.

11.2 Storage precautions

(1) When storing the LCD modules avoid exposure to direct sunlight or to the light of fluorescent lamps.
(2) The LCD modules should be stored within the rated storage temperature range. The recommend condition is: Temperature: 0 ~ 35 ℃ at normal humidity.
(3) The LCD modules should be stored in a room without acid, alkali or other harmful gas.

11.3 Transportation Precautions

The LCD modules should not be dropped or subject to violent mechanical shock during transportation. Also they should avoid excessive pressure, water, high humidity and direct sunlight.

11.4 Screen saver Precautions

Not display the fixed pattern for a long time. Use a screen saver, if the fixed pattern is displayed on the screen

11.5 Safety Precautions

(1) When you waste damaged or unnecessary LCDs, it is recommended to crush LCDs into pieces and wash t hem off with solvents such as acetone and ethanol, which should later be burned
(2) Be sure to turn off the power supply when inserting or disconnecting the LED backlight cable.
(3) LED driver should be designed to limit or stop its function when over current is detected on the LED.